TECHNOLOGY INDEPENDENT DEGRADATION OF MINIMUM NOISE FIGURE DUE TO PAD PARASITICS

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Abstract:

In order to investigate the influence of pad parasitics on device noise performance, noise parameters on Si CMOS, GaAs MESFET and GaAs p-HEMT transistors were determined. Measurements of devices with various gate widths demonstrate that the parasitic losses of the pads substantially influence the noise performance independent of FET technology. To accurately separate the noise contribution of the pad and the device, a noise parameter de-embedding procedure has been developed. It is shown that for an improvement of minimum noise figure NF_{min} of devices on non ideal substrates, pad losses must be minimized. Especially for small input transistors of amplifiers, pad parasitics must be considered during device modeling and design. A mathematical procedure using noise correlation matrices allows the embedding and de-embedding of noise parameters.

Introduction:

Since noise performance is an important design factor regardless of the technology used, improving the noise figure of a device is desirable. Using Si-CMOS as an example, the noise performance is investigated. Due to the significant losses at higher frequencies of silicon substrates, the device performance is limited [1], [2]. Earlier investigations [3], [4] have modeled and simulated the influence of lossy pads, but only for silicon technology.

Noise models for transistors commonly rely on measurements of large transistors and are scaled mathematically for other gate widths. If the noise contribution of the pads is not taken into account, this scaling can result in erroneous NF_{min} values for small transistors.

Based on measurements, this work shows that pad parasitics have significant influence on the minimum noise figure independent of FET technology, and different improvement possibilities are given. A method to accurately split the noise contribution of the transistor and the pads is presented.

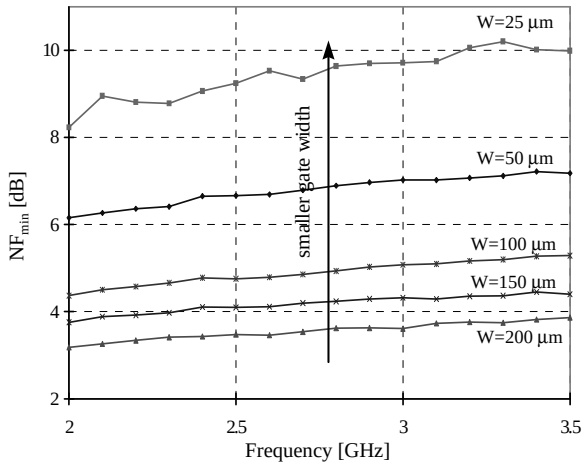

Figure 1: Measured minimum noise figure NF_{min} as a function of decreasing gate width W of CMOS transistors having a gate length of 0.25 µm and a constant current density of 100 mA/ mm.

Measurements:

Investigations on a 0.25 µm CMOS process with a low resistivity (4-6 Ω-cm) substrate have been performed. Noise parameters have been measured on transistors with various gate widths at the same current densities. As can be seen from Fig. 1, the minimum noise figure NF_{min} increases drastically as the gate width decreases.

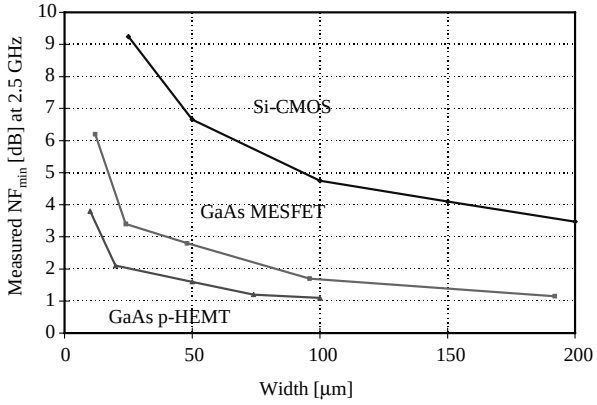

Figure 2: measured minimum noise figure NF_{min} at 2.5 GHz for various transistors as a function of gate width a) CMOS MOSFETs b) GaAs MESFETs and c) GaAs p-HEMTs.

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Similar measurements have been performed on GaAs devices for comparison. The GaAs MESFET has a gate length of 0.7 μm and the GaAs p-HEMT has a gate length of 0.35 μm.

Figure 2 shows the measured NF_{min} as a function of gate width at 2.5 GHz for MOSFETs, MESFETs and p-HEMTs. As the gate width of the transistors decreases, the measured minimum noise figure increases. This stands in contrast to theory where the minimum noise figure is independent of device scaling. The reason for the increase in NF_{min} is that smaller transistors have extremely high input impedances when compared to the impedances of the pad structures. Thus, the pad impedances begin to dominate the measurement results. Even in GaAs technologies (MESFET and p-HEMT) where pad losses are small, pad parasitics still influence the minimum noise figure as the transistors become smaller.

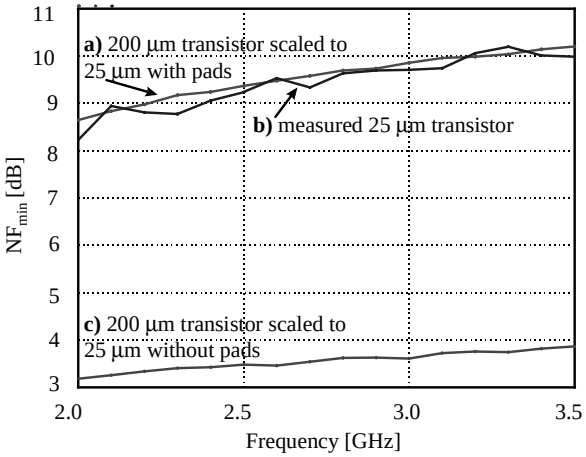

*Figure 3: NF_{min} of **a)** a 200 μm mathematically scaled to 25 μm: with pads, **b)** a measured 25 μm transistor and **c)** a 200 μm mathematically scaled to 25 μm: without pads.*

To demonstrate this effect, a 200 μm CMOS transistor was mathematically scaled to 25 μm and compared to actual measurements of a 25 μm transistor (Fig. 3 curves c and b). The simple scaling of a transistor to smaller gate widths produces an error of 5.5 dB at 2 GHz, because the measured NF_{min} of a 25 μm transistor is largely determined by the lossy pad structure. Thus, transistors must be de-embedded, scaled and then embedded to obtain accurate simulation results. This is demonstrated by adding a measured pad structure to the mathematically scaled 200 μm transistor (Fig. 3 curve a). Only this combination describes the noise performance of a 25 μm transistor correctly.

Noise de-embedding procedure:

To investigate the intrinsic noise performance of devices on lossy substrates, a noise de-embedding procedure has been developed. The procedure, based on the noise analysis of linear networks by [5], uses noise correlation matrices for calculation. As with S-parameter de-embedding procedures, large transistors provide reasonable accuracy for de-embedding of noise parameters [6].

The basic idea behind a de-embedding process is to mathematically subtract the influences of the extrinsic structure to obtain the intrinsic noise parameters. Thus, mathematical matrices called correlation matrices were developed [5].

Any noisy two-port can be replaced by a noise equivalent circuit which consists of the original two-port (noiseless) and two additional noise sources [7]. The three most common representations include the admittance, impedance and chain representations. A physically significant description of the noise sources is given by their self and cross-power and cross correlation functions. Arranging these spectral densities in matrix form leads to the noise correlation matrix [5]. Each representation has an electrical matrix (Y, Z, and A) and a corresponding correlation matrix as shown in Fig. 4.

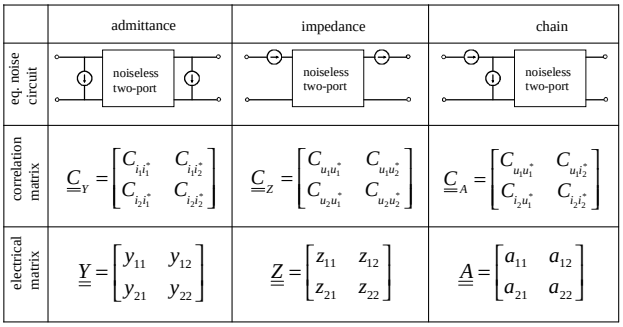

Figure 4:Two-port noise representations, correlation and electrical matrices

To transform a correlation matrix from one representation to the other we can use the transformation formula in Equation 1.

$$\underline{\underline{C'}} = \underline{\underline{T}}\,\underline{\underline{C}}\,\underline{\underline{T}}^{+} \qquad (1)$$

where $\underline{\underline{C}}$ is the original correlation matrix and $\underline{\underline{C}}$' is the resulting correlation matrix. The transformation matrix $\underline{\underline{T}}$ is given in Figure 5. and $\underline{\underline{T}}^{+}$ is the Hermitian conjugate (conjugate transpose). The $\underline{\underline{T}}$ matrix depends only upon the electrical matrix of the two-port.

For noise analysis of multiple two-ports either in series, in parallel or in cascade, the resulting matrices can be calculated as in Equations 2, 3, and 4 respectively.

$$\underline{\underline{C}}_Y = \underline{\underline{C}}_{Y1} + \underline{\underline{C}}_{Y2} \qquad \text{(parallel)} \qquad (2)$$

$$\underline{\underline{C}}_Z = \underline{\underline{C}}_{Z1} + \underline{\underline{C}}_{Z2} \qquad \text{(series)} \qquad (3)$$

$$\underline{\underline{C}}_A = \underline{\underline{A}}_1 \underline{\underline{C}}_{A2} \underline{\underline{A}}_1^+ + \underline{\underline{C}}_{A1} \qquad \text{(cascade)} \qquad (4)$$

where the subscripts 1 and 2 refer to the two-ports to be connected. The equations for series and parallel connections are relatively straight forward while the cascaded two-ports require both sources to be transformed to the input. Hence, the relation includes the electrical matrix of the first two-port.

resulting represenation	original represenation: admittance	impedance	chain
admittance	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$	$\begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}$
impedance	$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -z_{11} \\ 0 & -z_{21} \end{bmatrix}$
chain	$\begin{bmatrix} 0 & a_{12} \\ 1 & a_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -a_{11} \\ 0 & -a_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

Figure 5: Transformation matrices to calculate other correlation representations

Some restrictions do apply to these formulas. The noise sources of each of the basic two-ports are assumed to be uncorrelated. However, as long as the basic two-ports correspond to individual devices, the sources are indeed uncorrelated. Problems may arise in device modeling applications.

To begin de-embedding, the correlation matrix of both two-ports must be known. These matrices are obtained from theoretical considerations or noise parameter measurements. Usually, the correlation matrix of passive networks are calculated from theoretical considerations, i.e. thermal noise of network. The correlation matrices in impedance and admittance representations of such a two port are given in Equations 5 and 6.

$$\underline{\underline{C}}_Z = 2 \cdot k \cdot T \cdot \Re\left\{\underline{\underline{Z}}\right\} \qquad (5)$$

$$\underline{\underline{C}}_Y = 2 \cdot k \cdot T \cdot \Re\left\{\underline{\underline{Y}}\right\} \qquad (6)$$

The correlation matrix is completely determined by the real part of their electrical matrix and the absolute temperature T.

In some cases, the correlation matrix can not be derived from theory. Noise parameter measurements provide the required information. R_n, NF_{min}, and Y_{opt} are usually used to determine the correlation matrix as in Eq. 7. For more information on noise parameters, the reader is referred to [8], [9]. Equation 7 is slightly different from [5] due to a typographical error in [5]. This error has been corrected and confirmed by [10].

$$\underline{\underline{C}}_A = 2 \cdot k \cdot T \cdot \begin{bmatrix} R_n & \frac{F_{\min}-1}{2} - R_n \cdot Y_{opt}^* \\ \frac{F_{\min}-1}{2} - R_n \cdot Y_{opt} & R_n \cdot \left|Y_{opt}\right|^2 \end{bmatrix} \qquad (7)$$

where T is the absolute temperature, R_n is the equivalent noise resistance, F_{min} is the minimal noise figure (linear) and Y_{opt} is the optimal source admittance.

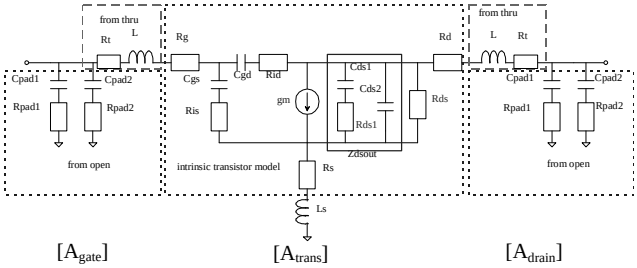

Figure 6: Small signal equivalent circuit model of the measured structure and the corresponding electrical matrices required for de-embedding

To obtain the intrinsic noise parameters of a transistor, a de-embedding procedure must be performed. A chain matrix for the intrinsic transistor can be calculated from the intrinsic S-parameters. For the external structure, its small signal model can be transformed into a chain matrix for both the gate and the drain side. Thus, the electrical matrices for a cascade of three two-ports (Fig. 6) are all known. The electrical chain matrices are given in Equations 8 and 9.

$$\underline{\underline{A}}_{gate} = \begin{bmatrix} -1 & -(j\omega L + R_t) \\ -Y_{open} & -Y_{open} \cdot (j\omega L + R_t) - 1 \end{bmatrix} \qquad (8)$$

$$\underline{\underline{A}}_{drain} = \begin{bmatrix} -Y_{open} \cdot (j\omega L + R_t) - 1 & -(j\omega L + R_t) \\ -Y_{open} & -1 \end{bmatrix} \qquad (9)$$

where

$$Y_{open} = \frac{s^2(C_{pad1}\tau_2 + C_{pad2}\tau_1) + s(C_{pad1} + C_{pad2})}{\tau_1\tau_2 s^2 + (\tau_1 + \tau_2)s + 1} \qquad (10)$$

and τ_1 and τ_2 are $C_{pad1}*R_{pad1}$ and $C_{pad2}*R_{pad2}$ respectively.

These chain matrices were calculated from their corresponding admittance matrices. Thus, the correlation matrices of both the gate and drain two-ports can be written using Eq. 6. Once $\underline{\underline{C}}_{Yg}$ and $\underline{\underline{C}}_{Yd}$ are determined, the corresponding chain representations $\underline{\underline{C}}_{Ag}$ and $\underline{\underline{C}}_{Ad}$ can be calculated using Eq. 1 where $\underline{\underline{T}}$ is the admittance to chain transformation from Fig. 5.

The correlation matrix $\underline{\underline{C}}_{Atot}$ for the complete structure is determined from the noise parameter measurements using Eq. 7. Since the total structure is a cascade of three two-ports, the de-embedding procedure needs to be performed twice to obtain the intrinsic correlation matrix $\underline{\underline{C}}_{Atr}$.

Equation 11 performs the total de-embedding procedure by applying inverse of Eq. 4 twice.

$$\underline{\underline{C}}_{Atr} = \underline{\underline{A}}_{gate}^{-1}\left[\underline{\underline{C}}_{Atot} - \underline{\underline{C}}_{Ag}\right]\underline{\underline{A}}_{gate}^{+^{-1}} - \underline{\underline{A}}_{trans}\underline{\underline{C}}_{Ad}\underline{\underline{A}}_{trans}^{+} \quad (11)$$

By applying Eq. 7 to $\underline{\underline{C}}_{Atr}$, the intrinsic noise parameters R_n, NF_{min} and Y_{opt} are determined.

In any technology, the minimum noise figure degrades when measuring small devices. Even though NF_{min} theoretically remains constant when scaling device widths, such degradations are extremely obvious when measuring low resistivity Si-CMOS transistors.

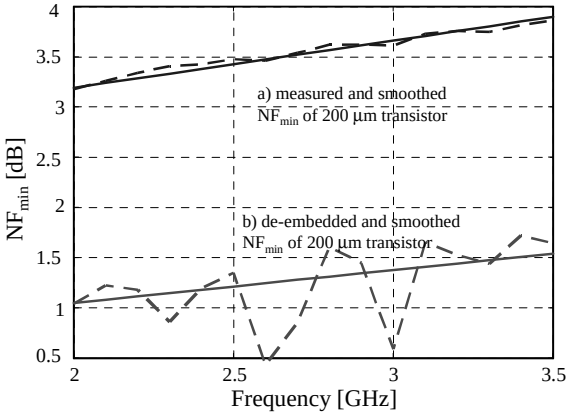

Figure 7: measured and smoothed NF_{min} of a 200 µm transistor, a) with pads, b) de-embedded (without pads).

As is shown in Fig. 7, the measured and smoothed minimum noise figures are clearly different for a 200 µm CMOS transistor with the pads taken into account and with the pads de-embedded. Even for such a large device, the lossy pads degrade the minimum noise figure by 2 dB at 2 GHz. The intrinsic device under these bias conditions has an NF_{min} of 1.1 dB. We can therefore conclude that for significant improvement in the usable minimum noise figure NF_{min}, the losses of the input pads need to be minimized.

A few possible solutions to minimize the influence of pad parasitics include: (1) on-chip matching to reduce the impedance level seen at the pads, (2) shielding of the pads as in [3], (3) smaller input pad to reduce parasitics and (4) either a higher resistivity (semi-insulating) or an extremely low resistivity (epitaxial layer with highly doped bulk layer) substrate ([3], verified by our own measurements).

A combination of the suggested changes such as a smaller pad using the top metal layer shielded by the bottom grounded metal layer may prove to be the best solution since no major process changes are required. The additional capacitance (purely reactive) may then be used for matching of the input stage of a low noise amplifier.

Conclusion:

Pad parasitics influence the noise performance of small transistors with high input impedances independent of FET technology. Especially for CMOS transistors on low resistivity substrates, lossy pads dramatically increase minimum noise figures of the devices. To accurately split the pad parasitics from the intrinsic devices, a noise de-embedding procedure has been presented. As a result, the intrinsic NF_{min} of a CMOS transistor is shown to be 1.1 dB at 2 GHz compared to 3.2 dB for the same device with pads. To improve the overall useable noise performance, the losses of the pad parasitics must be minimized. With such improvements, CMOS LNAs on low resistivity substrates may soon become a strong competitor of GaAs LNAs in the lower GHz region.

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